

ABSTRACT OF THE DISCLOSURE

5 A SONET multiplexed system architecture that permits  
greater levels of integration. The system architecture  
includes a time slot interchanger for routing information  
from at least one SONET input signal path associated with  
a respective first time slot to at least one SONET output  
signal path associated with a respective second time  
slot. Each SONET input signal path includes a pointer  
interpreter, and each SONET output signal path includes a  
10 FIFO buffer serially coupled to a pointer generator. The  
system architecture further includes a synchronization  
buffer included in the SONET input signal path and  
configured to transfer the input signal to the clock rate  
of the time slot interchanger. The system architecture  
15 permits greater levels of integration when the time slot  
interchanger has more inputs than outputs, and/or the  
time slot interchanger provides the output signal to a  
pointer processor to transfer the output signal to the  
clock rate of the SONET output signal path.  
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